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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,444	01/30/2004	Xiaoming Jiang	ASAM.0099	7243

7590 07/28/2005

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,444	JIANG ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/04 & 3/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 1/30/2004. Claims 1-16 are presented for examination.

The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This **request** does not require applicant to perform a search. This request is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is

most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 1-16 are objected to because of the following informalities:

As per claims 1,8, and 15, the term --these units-- (claim 1, line 4; claim 8, line 3; and claim 15, line 4) should be amended to --the channel control units-- in order to properly distinguish between the channel control units and the disk control units. Likewise the term --these units-- should be amended to --the disk control units-- (claim 1, line 7; claim 8, line 6; and claim 15, line 7) in order to properly identity the --units-- as --disk control units--.

Further regarding claim 1, line 18, the Examiner recommends amending the term --more than one of said data buses-- to --one or more of the said plurality of data buses-- as the Applicant later claims in claim 3 that a single one of the data buses can be utilized. Claims 8 and 15 recite similar limitations that claim that one or more of the data buses can be used.

As per claims 2 and 9, the Examiner recommends amending the phrase --said access request is set to upper 32 bits-- to --said access request is set in the upper 32 bits--, or the like, in order to more clearly define the limitation.

As per claims 3,5-7,10, and 12-14, the Examiner recommends amending the term --said reference data length-- to --said predefined reference data length-- since only the latter term is defined in parent claims 3 and 10.

As per claim 5, the Examiner recommends amending line 11 to read "...said reference data length, the data transfer integrated circuit uses one of said data buses for each of the access requests to thereby" in order to clarify the limitation.

As per claims 6 and 13, the Examiner recommends amending line 4 to read "data length, and when both of said two data buses ..." in order to clarify the limitation. Further, the Examiner recommends amending the term --out of use-- to --available--, --idle--, or the like, in order to clarify the claim.

As per claims 7 and 14, the Examiner recommends amending line 3 to read "... data length, and when any one of said two data buses ..." in order to clarify the limitation. Further, the Examiner recommends amending the term --out of use-- to --available--, --idle--, or the like, in order to clarify the claim.

As per claim 12, the Examiner recommends amending line 11 to read "... selecting one of said data buses for each of the access request" in order to further clarify the claim.

As per claim 15, the Examiner recommends amending line 20 to read "... said second controller occurs from any one ..." in order to clarify the limitation. Examiner recommends amending line 21 to read "... said disk control units and said CPU, of the first controller ..." in order to convey that the access request occurs from a control unit, a disk control unit, or the CPU of the first controller, thereby clarifying the claim. Further the Examiner recommends amending the term --toward-- (line 21) to --to-- for clarity. Further the Examiner recommends amending the phrase "... which requests sets therein an access type ..." of lines 22-23 to read "... to which the access request contains therein an access type ..." or the like in order to clarify the limitation. Still further, the Examiner recommends amending line 24 to read "... disk control units of from said CPU of the first controller, and" in order to convey which controller's elements are producing the access request. Finally, the Examiner recommends amending line 29 to read "said access type that is contained within the access request." in order to clarify the limitation.

As per claim 16, the Examiner recommends amending line 4 to read "...said cache memory of the second controller when said access type being ~~set in said~~ contained within the" or the like in order to convey which cache memory (i.e. the first controller's or second controller's is being accessed. Further, the Examiner recommends amending line 7 to read "control units of the first controller and, when said access type being ~~set~~ contained ..." in order to clarify the limitation. Finally, the Examiner recommends amending line 8 to read "request from said CPU of the first controller, the second controller uses a single one ..." in order to further clarify the limitation.

Claims 4 and 11 are objected to as being dependent on objected claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-7 and 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 2 and 9, the term --said bus-- is vague and open to multiple interpretations. It is not immediately clear if the term --said bus-- refers to the --more than one bus-- of the parent claim or if --said bus-- refers to a single one of the --more than one bus--. It is the duty of the Applicant to particularly point out and distinctly claim the subject matter which Applicant regards as his invention. Nonetheless, for the purposes of examination, the Examiner shall regard all of the buses of the --more than one bus-- to be PCI buses.

As per claims 3 and 10, the claims are silent with respect to the instant case when the --transfer data length-- is *equal* to the predefined reference data length. Nonetheless, for the purposes of examination, the Examiner shall interpret the claim such that the data transfer integrated circuit uses ***one*** of the data buses to access the cache memory when the access request is shorter *or equal* to the predefined reference data length.

Claims 4-7 and 11-14 are rejected as being depended on rejected claim 3 and 10, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3,4,8,10,11,15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujibayashi et al. (U.S. Patent Application Publication No. 2002/0169901) in view of Goldrian et al. (U.S. Patent No. 5,872,944).

As per claims 1, 8, and 15 Fujibayashi shows in figure 3 a plurality of hard drives 102, a plurality of channel control units 103 for performing data transfer and reception (¶73) between the channel control units and a plurality of information processing apparatuses 101 through a storage area network (520 figure 5), a plurality of disk control units 104 for performing data transfer and reception between the disk control units 104 and the hard drives 102, a CPU 412 for performing --control-- of the plurality of channel control units and the disk control units (¶¶39-40), a cache memory 108 for storage of data being transferred and received between the channel control units 103 and the disk control units 104 (¶73), a data transfer integrated circuit (herein DTIC) 106, which is shown being coupled via a plurality of buses to the disk control units 104, the channel control units 103, and the CPU 412 (figure 4). Fujibayashi does not specifically show the DTIC connected to the cache 108 via multiple buses. Goldrian teaches a dual-bus approach to cache/processor interaction wherein the dual-bus structure is operable such that the bus bandwidth can be expanded in one direction when a larger transaction requires larger

bandwidth than a single bus can provide (abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the storage area network of Fujibayashi with the dual-bus teaching of Goldrian in order to have dynamically increased the bandwidth to and from the cache memory 108 from the DTIC 106 for large instruction. Such a modification to Fujibayashi would have increased the access speed of the cache 108 for store and fetch instructions (column 5, line 64 - column 6, line 5). Further advantages of the teachings of Goldrian produce a reduction in hardware expense (column 6, lines 56-61).

Access requests from the channel control units and the disk control units to the cache (¶73) are fulfilled by the DTIC of modified Fujibayashi according to the teachings of Goldrian. The transfer data length determines whether or not the cache memory is accessed via the dual-bus architecture or a single bus (column 5, line 64 - column 6, line 5). Accesses involving a larger transfer data length utilize both buses (column 7, lines 3-24) and are detected via a transfer length and specific command indications (figures 7-9A). It should be noted that while the Goldrian reference teaches the dual-bus architecture between a processor and cache, the Examiner is simply combining the teaching of the logic required to implement the cache access using a dual-bus of Goldrian to the DTIC 106 of Fujibayashi, as the DTIC is the element responsible for accessing the cache 108.

Further regarding claim 15, figure 3 of Fujibayashi shows a first controller (unit disk controller #1) and a second controller (unit disk controller #2) each controller comprises channel control units 103, disk control units 104, a CPU (processor portion) for controlling the channel control units and disk control units (¶73), cache memory 108, and a DTIC 106 with each

controller's DTIC communicably connected via network 310. The DTICs transfer data requests as shown in figure 5. Goldrian shows an access type (CMD and ID fields) in figure 7 that is associated with access requests. A Store command (figure 7) contains such fields since the store command includes a specified amount of data (704-707), which indirectly indicate that the request has come from one of the channel control units since all requests arrive via the channel control units since the access requests of the information processing apparatuses are received by the channel control units. The number of buses utilized when accessing the cache of the second controller is determined by the access type as discussed above with respect to the access request ID and CMD fields (fetch and store accesses utilize both buses - column 5, line 64 - column 6, line 5).

As per claims 3, 10, and 16, Goldrian shows two data buses in figure 6A and 6B (600 and 601). The Examiner is considering a --predefined transfer length-- to be a single bus cycle. As shown in figures 6A and 6B, when a request that [is smaller or] equal to the predefined reference data length, the DTIC utilizes only a single bus of the dual-bus architecture to access the cache. The transfer data length is inherently encoded since, as shown in figures 6A and 6B, the access request includes a request ID and CMD fields, which indirectly indicate the transfer data length of the access as they indicate the type of command forthcoming. When a transfer data length is longer, the DTIC utilizes both buses, as shown in figure 7.

As per claims 4 and 11, Fujibayashi shows in figure 3 multiple (two) cache memory portions that comprise the cache 108. In an alternative, Goldrian states in column 11, lines 56-67, that an L1 is accessed first in order to try and retrieve data for a fetch command and only if a miss occurs, is the L2 accessed (utilizing the dual-bus architecture). Thus the Examiner is

considering the --cache memory-- to be the combination of the L1 and L2 caches (two physically separate caches) and the L2 is communicably connected via the data buses to the DTIC, as shown in figures 6-13.

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujibayashi et al. (U.S. Patent Application Publication No. 2002/0169901) in view of Goldrian et al. (U.S. Patent No. 5,872,944), as applied to claims 1,3,4,8,10,11,15 and 16 above, in further view of *The Microsoft Computer Dictionary* (herein Microsoft).

Modified Fujibayashi does not specifically teach the buses connected to the DTIC as being PCI buses. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented the bus architecture of Fujibayashi as PCI buses. Microsoft teaches that utilizing a PCI bus architecture would have allowed for PCI adapters to perform concurrent tasks, thereby increasing the bandwidth and processing speed of modified Fujibayashi. Microsoft teaches on page 395 that the PCI bus can have a 64-bit width. Goldrian shows that the transfer data length is set in the address phase (elements 702 and 703). The transfer data length is inherently encoded since, as shown in figures 6A and 6B, the access request includes a request ID and CMD fields, which indirectly indicate the transfer data length of the access as they indicate the type of command forthcoming.

Allowable Subject Matter

Claims 5-7 and 12-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claims 5 and 12, the prior art of record does not specifically teach each claimed limitation of claims 5 and 12.

Claims 6,7,13, and 14, would be allowable, as they are dependent on claims 5 and 12.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hewitt (U.S. Patent No. 6,202,116) teaches a system using dual-buses that can be utilized singly or in combination to increase system bandwidth.

Tanaka et al. (U.S. Patent Application Publication No. 2002/0099901) teaches a SAN architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

HONG CHONG KIM
PRIMARY EXAMINER